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# Analog Neurons that Signal with Spiking Frequencies

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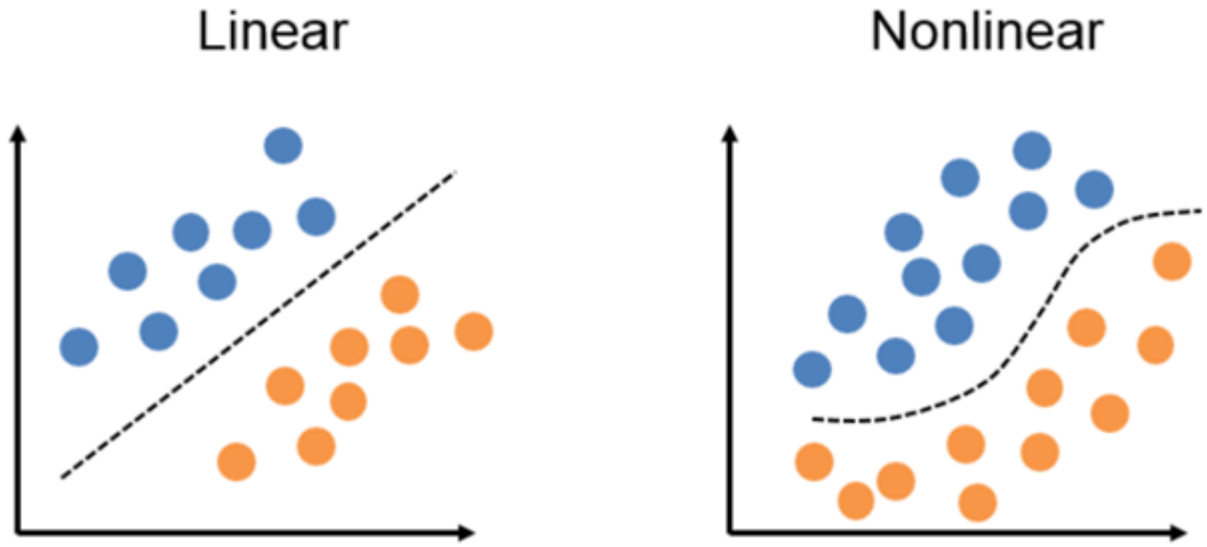
BioRC
**Bio**mimetic
**R**eal-time
**C**ortex

# Introduction

- Adaptive synaptic frequency filtering has been found in the region of fore-brain such as hippocampus. [1]
- The adaptive synaptic frequency filtering provides nonlinear signal processing besides threshold function of neurons. [2]
- The plasticity changing rules of the adaptive synaptic frequency filtering are still unclear, we proposed a STDP-like method here to explore the possible learning methods.


[1] Vitaly A Klyachko and Charles F Stevens. Excitatory and feed-forward inhibitory hippocampal synapses work synergistically as an adaptive filter of natural spike trains. *PLoS biology*, 4(7):e207, 2006.

[2] Stephen J Martin, Paul D Grimwood, and Richard GM Morris. Synaptic plasticity and memory: an evaluation of the hypothesis. Annual review of neuroscience, 23(1):649–711, 2000.

# Outlines

- Voltage dependent variable-frequency axon hillock circuit
- Frequency sensitive synapse circuit with memristor
- STDP-like learning implementation circuit
- Frequency adaptive synapse
- Frequency adaptive synapse with strength variation
- Alternative all CMOS frequency-selective synapse

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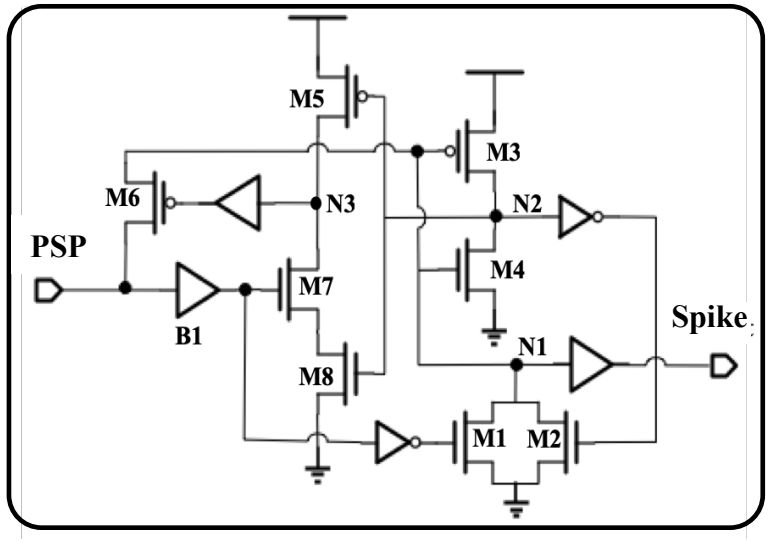
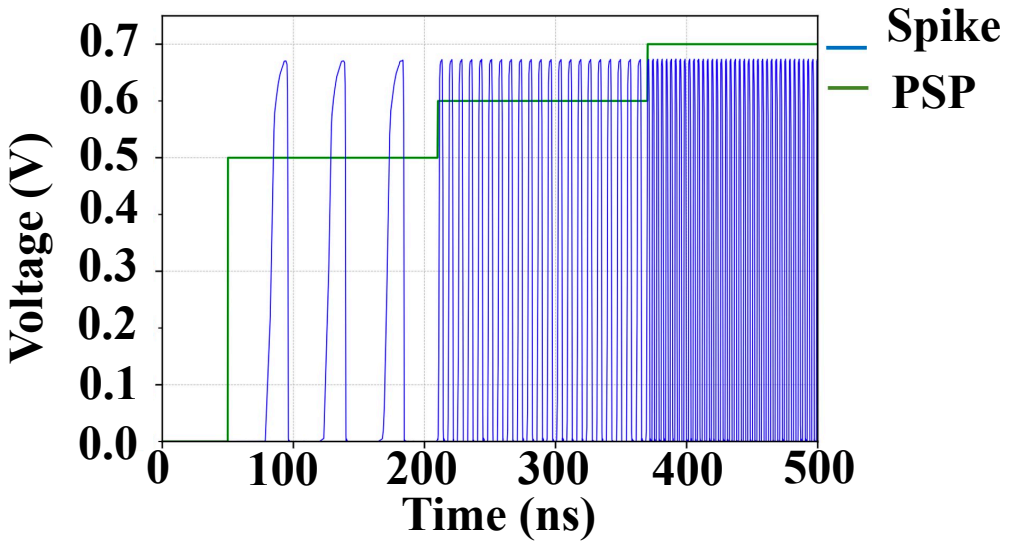
# Voltage dependent variable-frequency axon hillock

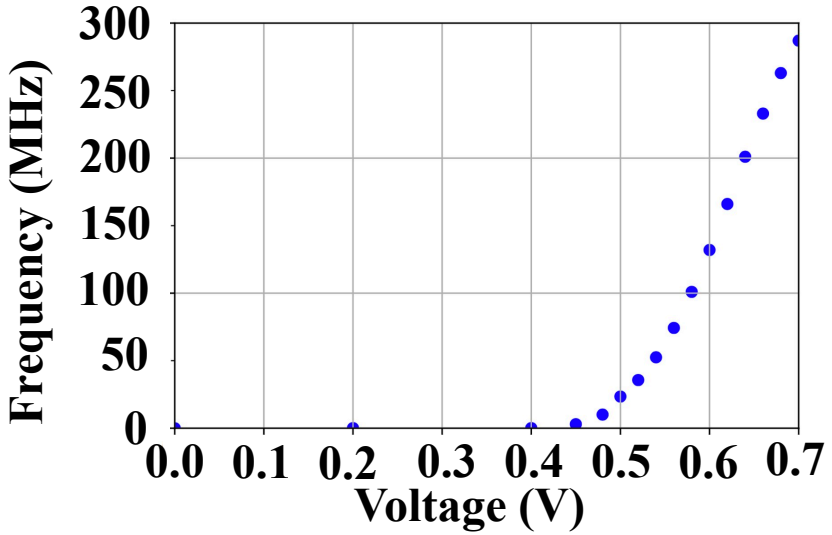
- This axon hillock converts the amplitude of PSP input above threshold to firing frequency linearly.
- Due to the transistor M6 is operating in linear region, the frequency of the output spike train is linearly related with input voltage above threshold.

$$I_{SD} = \mu_p C_{ox} \frac{W}{L} \left[ (V_{SG} - |V_T|) V_{SD} - \frac{{V_{SD}}^2}{2} \right]$$




Output spike with Different PSP Level, When PSP level are 0.5V, 0.6V and 0.7V, output spike frequency are 20MHz, 130MHz and 280MHz correspondingly.




Linear relationship between PSP and firing frequency

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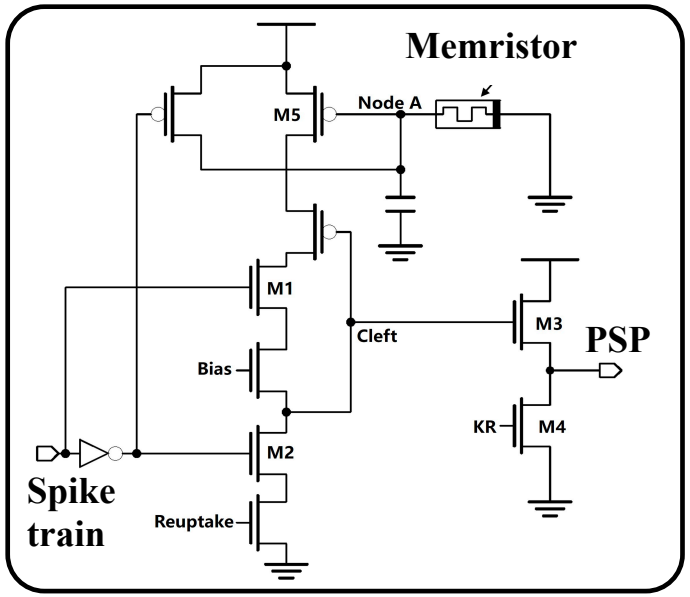
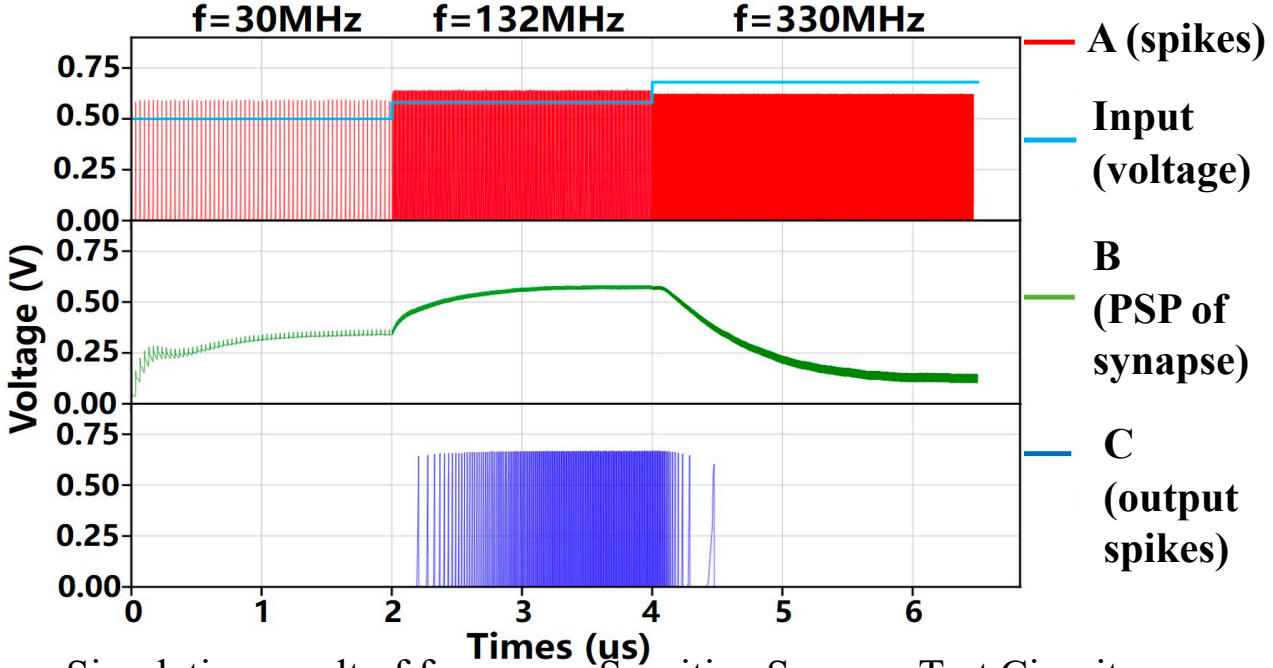
# Frequency sensitive synapse with memristor

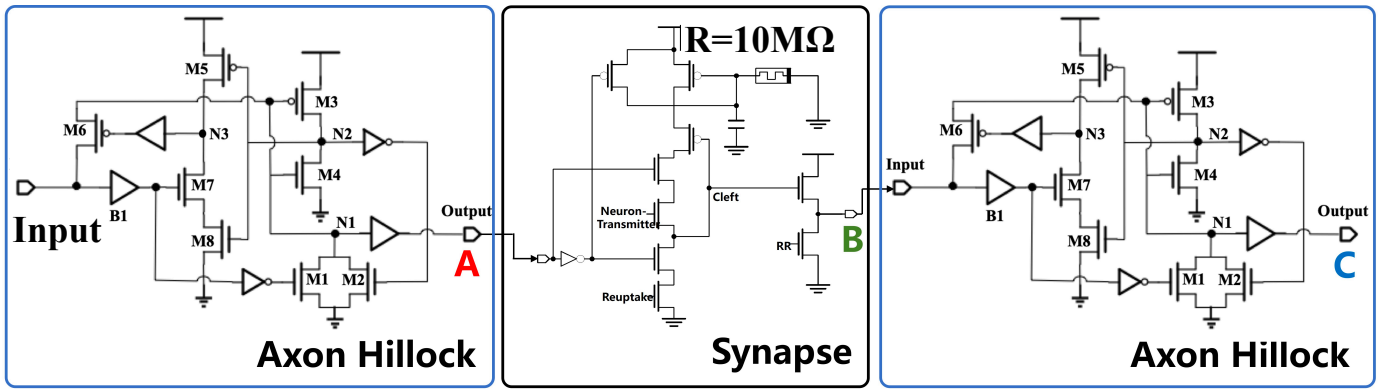
Memristor is used as variable resistor in this circuit



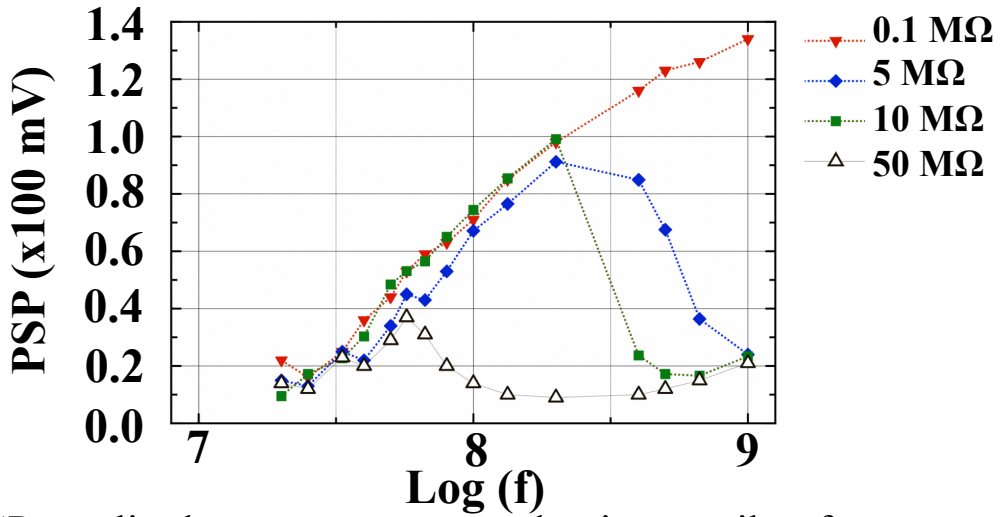

Circuit of frequency sensitive synapse




Simulation result of frequency Sensitive Synapse Test Circuit




Frequency Sensitive Synapse Test Circuit




PSP amplitude response respected to input spikes frequency

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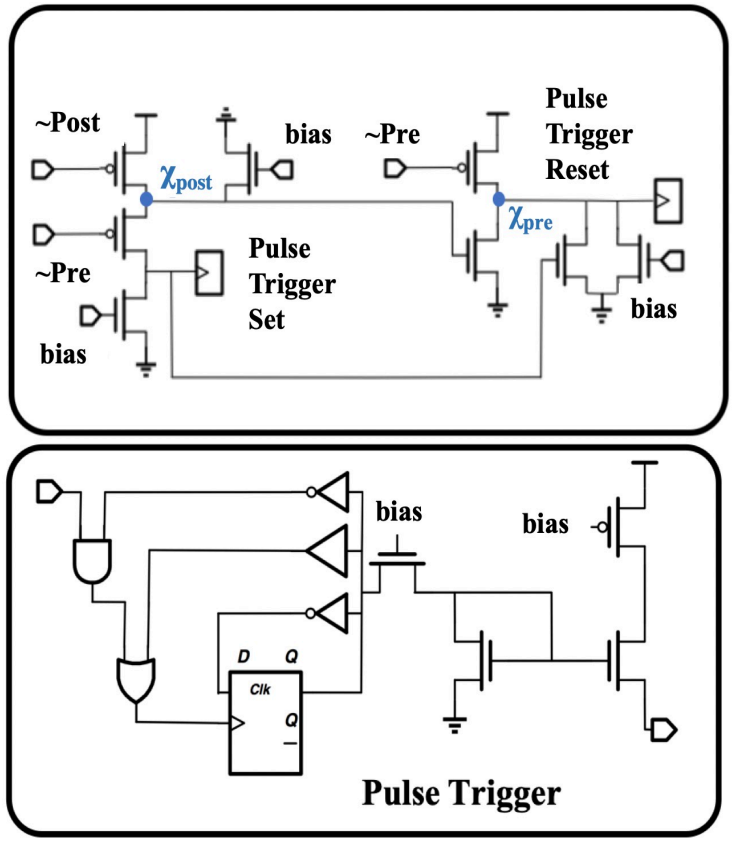
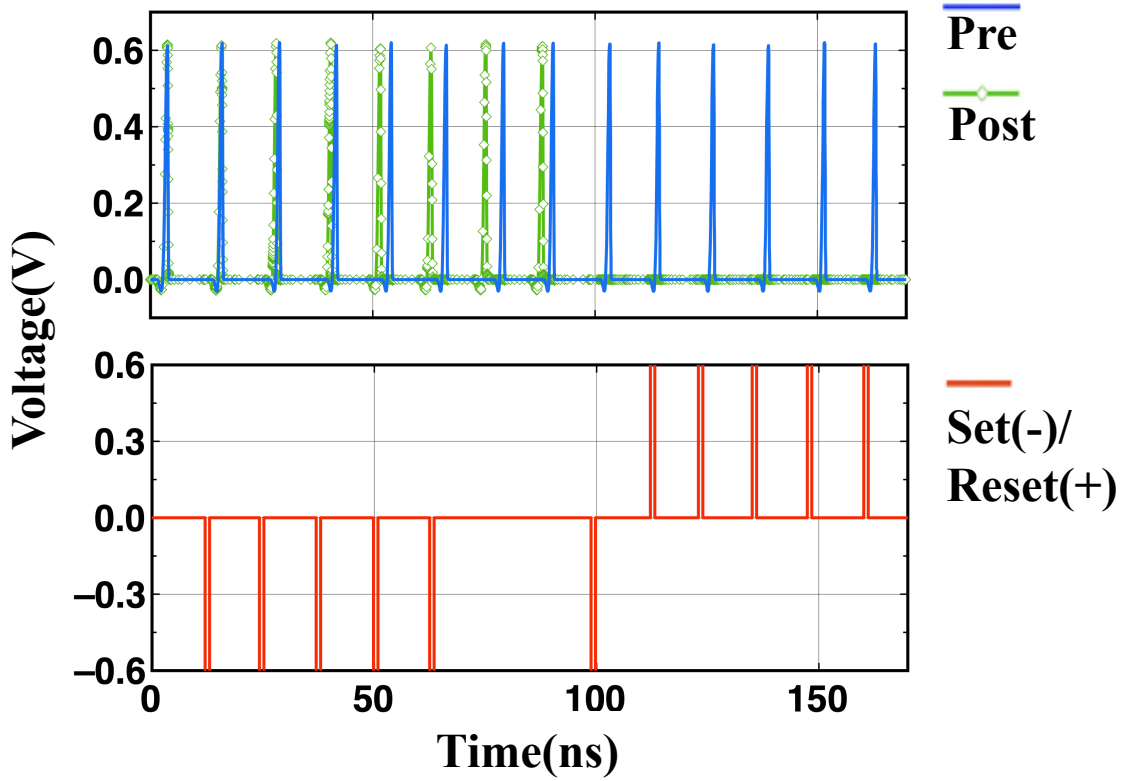
# STDP-like learning implementation circuit

STDP-like learning algorithm is implemented as:

- Post-Pre pair inside time window → Set (decrease resistance)
- Post-Pre pair outside time window → Null
- Only Pre spike → Reset (increase resistance)




STDP-like learning implementation circuit




Simulation Result of STDP-like learning

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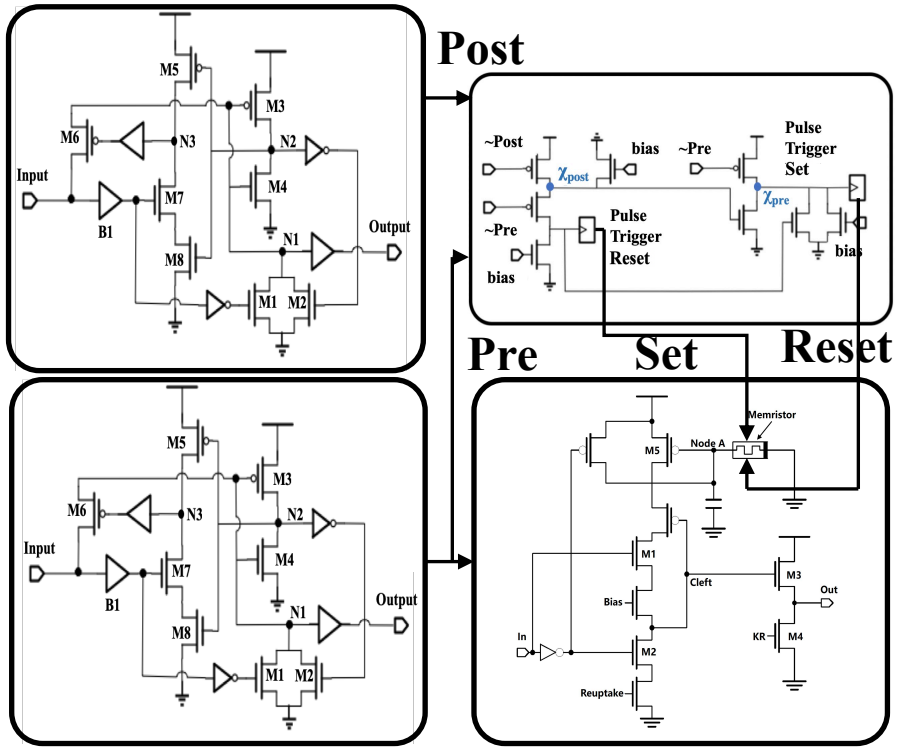
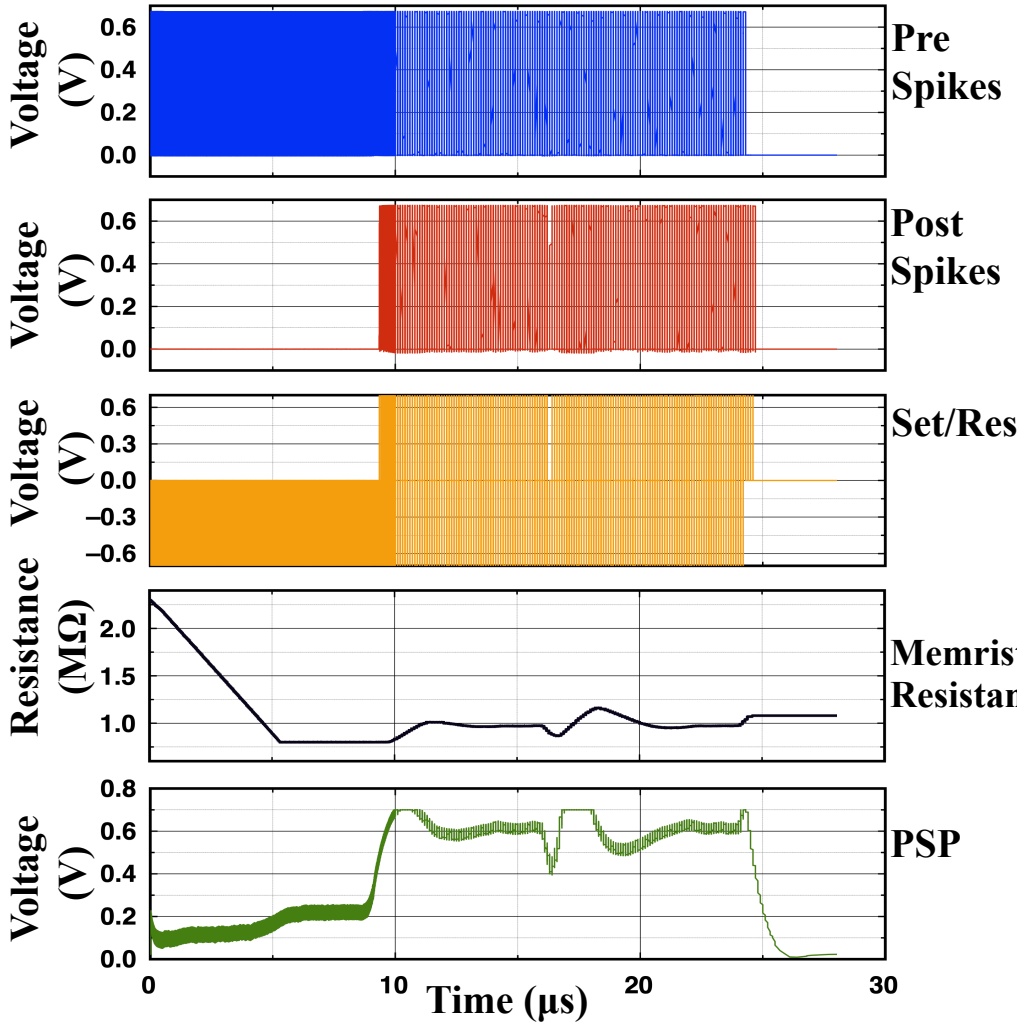
# Frequency adaptive synapse

- The STDP-like circuit tunes the resistance of memristor to select different frequency range.
- Two voltage dependent axon hillocks with given inputs provides *pre* and *post* spikes to test this frequency adaptive synapse.




Frequency adaptive synapse test circuit




The pre spikes fire in 300MHz for first 8µs and then in 130MHz, the post spikes fire in 300MHz from, the initial value of the memristor resistance is 2.8 MΩ and its minimum value is 800kΩ.

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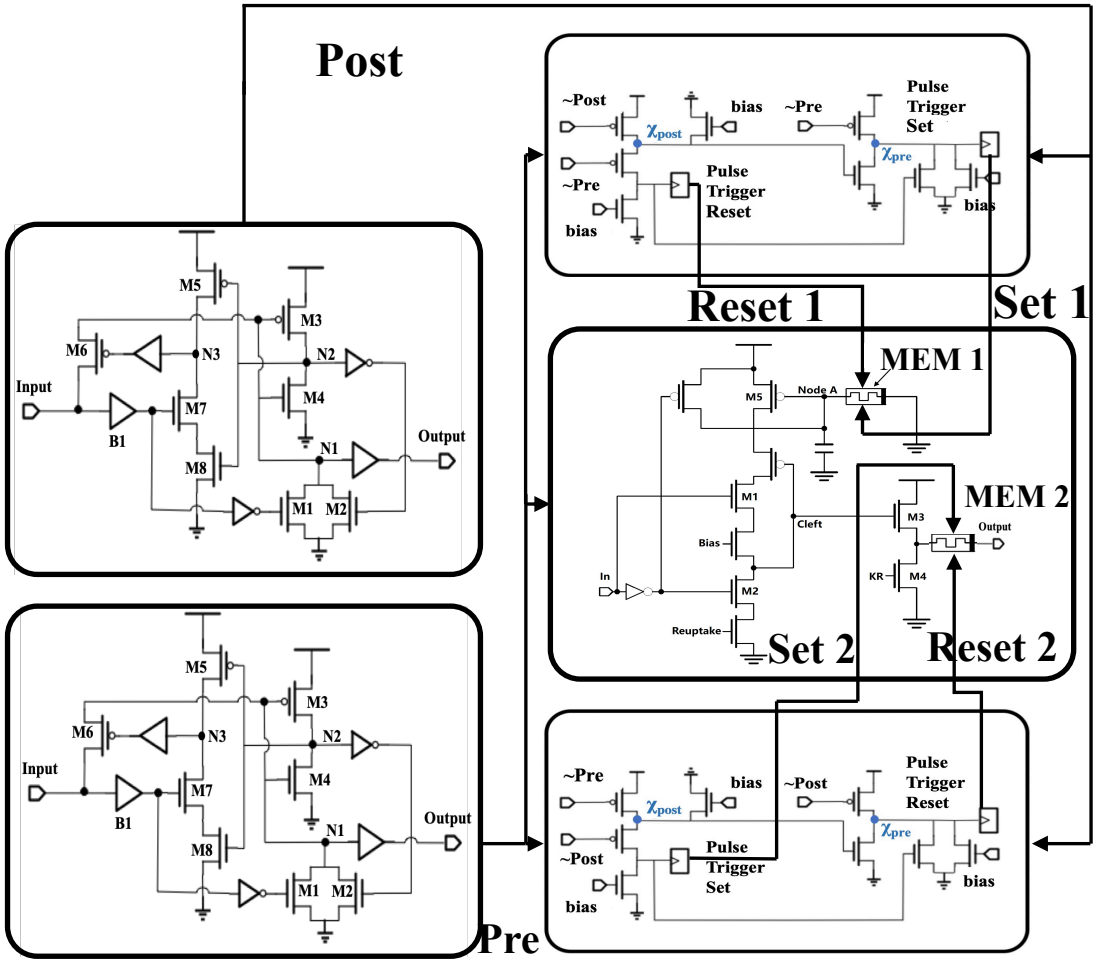
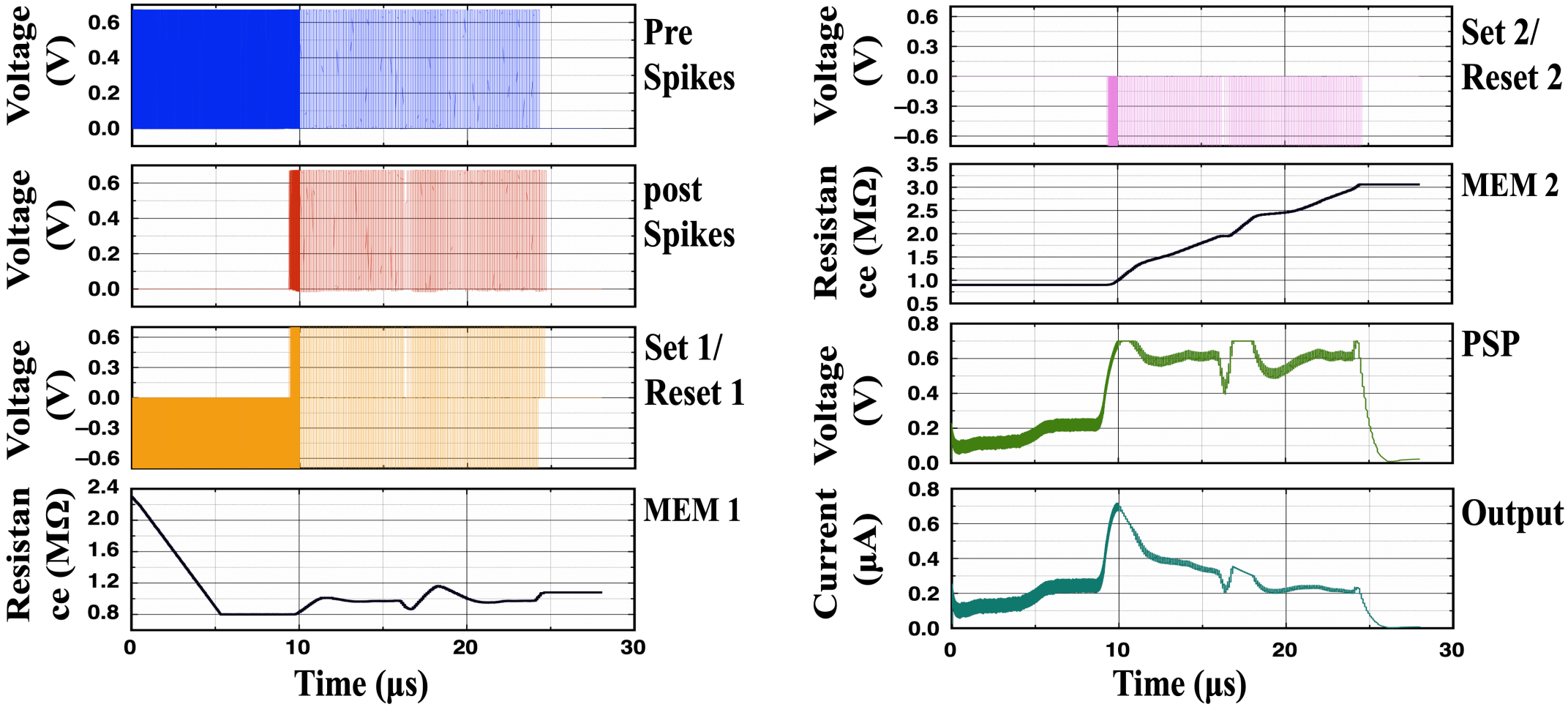
# Frequency adaptive synapse with strength variation

- Another memristor MEM2 is added after PSP of synapse
- Another STDP-like circuit is added to change the resistance of MEM2
- New STDP-like circuit follows Hebbian rule: Pre-Post → Strengthen (decrease resistance); Only post → Weaken (increase resistance)
- Same Pre and Post are fed into two STDP-like circuit




Frequency adaptive synapse with strength variation test circuit

# Frequency adaptive synapse with strength variation




Frequency adaptive synapse with strength variation test circuit simulation result. The pre spikes fire in 300MHz for first 8μs and then in 130MHz, the post spikes fire in 300MHz, the initial value of the MEM1 and MEM2 resistance are 2.8 MΩ and 800kΩ, the minimum value of memristor resistance is 800kΩ.

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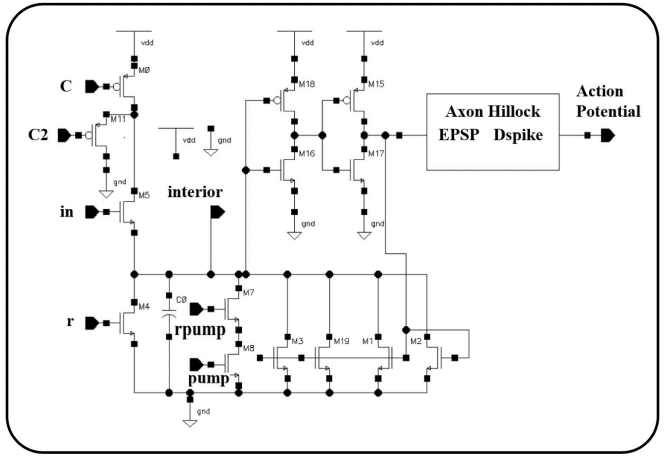
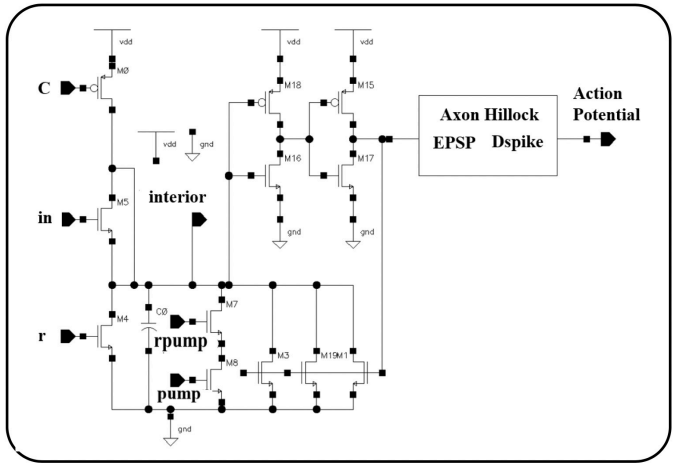
# Alternative all CMOS frequency-selective synapse

The frequency selective synapse also can be implemented by CMOS completely with dedicated design to reduce the fabrication complexity.



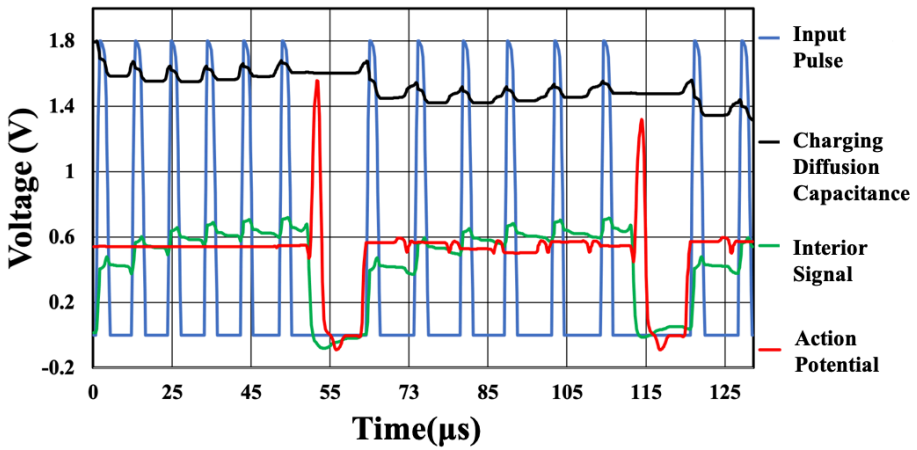

**(a)**

Low frequency synapse all CMOS circuit

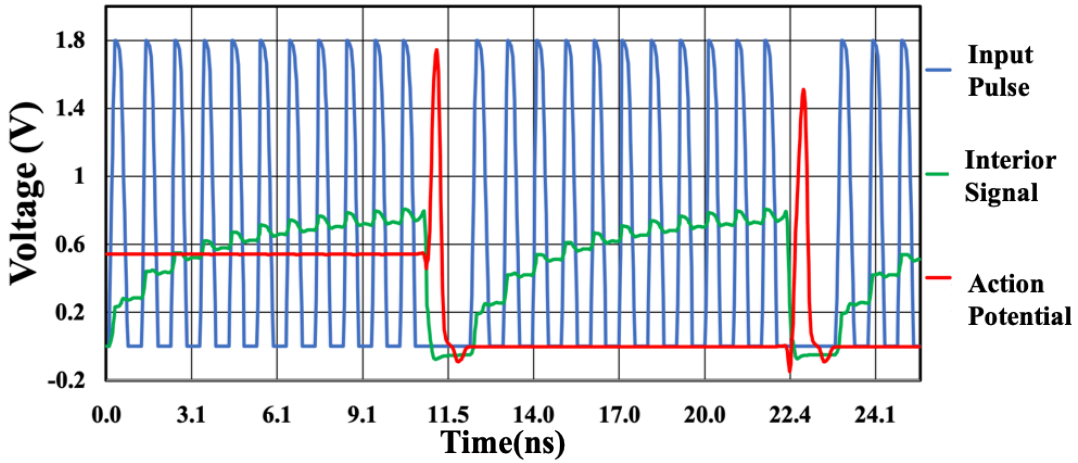



**(b)**

High frequency synapse all CMOS circuit




Low frequency synapse All CMOS circuit simulation result With 100Hz input




High frequency synapse All CMOS circuit simulation result With 1GHz input

# Conclusion

- In this work, we presented analog neuromorphic circuit designs of **voltage dependent variable-frequency axon hillock** and **frequency adaptive synapse**. We also proposed a STDP-like plasticity-changing rule to demonstrate a new **frequency learning** protocol along with a weight learning protocol (Hebbian learning).

- Both the linear function represented by strength plasticity and the **nonlinear function** represented by frequency plasticity are integrated in this synapse design. With this more complete synapse and the voltage dependent axon hillock, more complicated functions are expected to be learned through a simpler neuronal network structure. Moreover, the upper complexity limitation of target nonlinear functions is expected to be increased.

- In the future, we will explore complex nonlinear functions trained in a much simpler neural network structure.

# Acknowledgement

Lifelong Learning Machines (L2M) Project


Questions?