DANNA2: Dynamic Adaptive Neural Network Arrays

J. Parker Mitchell, Mark E. Dean, Grant R. Bruer, James S. Plank, Garrett S. Rose



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Last Year – A Robot with DANNA





DANNA2 Model Overview

- Programmable Leaky Accumulate & Fire neurons
- Neurons include accompanying synapses (no synapse chains)
- Lookup based Synaptic Plasticity (STDP)
- Discrete integer time steps
- All fires at time *t* are simultaneous
- Two Array Types
 - Grid Arrays A fixed grid of programmable elements with 5×5 nearest neighbor connectivity
 - Sparse Arrays A directed graph of connected elements (not runtime configurable)

The DANNA2 Element

- Built of small components
 - Programming Interface
 - Delay/Distance Registers
 - Synapse Table
 - Synapse Units with plasticity
 - Accumulator
 - Compare and Fire
 - Sub-cycle Counter
- Configurable and Extensible
- Capable of running at 250MHz on FPGAs



Figure 1: DANNA2 Element

Software Simulation

- Before simulation begins, create a network and queue inputs
- Check for incoming fires for time *t*
- Process internal fires for time t
- Schedule new fires after time *t* is fully processed
- Log fires from designated outputs
- Stop the simulation once desired time is reached



Figure 2: Simulation Flow

Performance Comparison

- Simple pass-through network to compare simulation performance
- Staggered firing pattern across all inputs
- Under 120 inputs, DANNA2 is $> 10 \times$ faster than DANNA
- At 7500 inputs, DANNA2 is 4.8× faster than DANNA



Figure 3: Benchmark Results

Example Application: Robonav



Future Work

- VLSI design and fabrication?
- Multi-chip scaling of arrays
- Embedded robotic deployment NeoN 2
- Investigation of leak and learning parameters
- Examine importance of precision in parameters
- Development of other hardware implementations including an event driven processor

Conclusion

- DANNA2 delivers an order of magnitude higher execution speed than DANNA in both hardware and software
- Additional speed and capability can be utilized to improve training performance
- Improves effective density compared to DANNA
 - 60% more usable neurons than DANNA on the same FPGA
 - Sparse arrays allow for optimized deployments
- Designed to be scalable and allow for new implementations

Acknowledgments



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